CORTLAND I/O Timing

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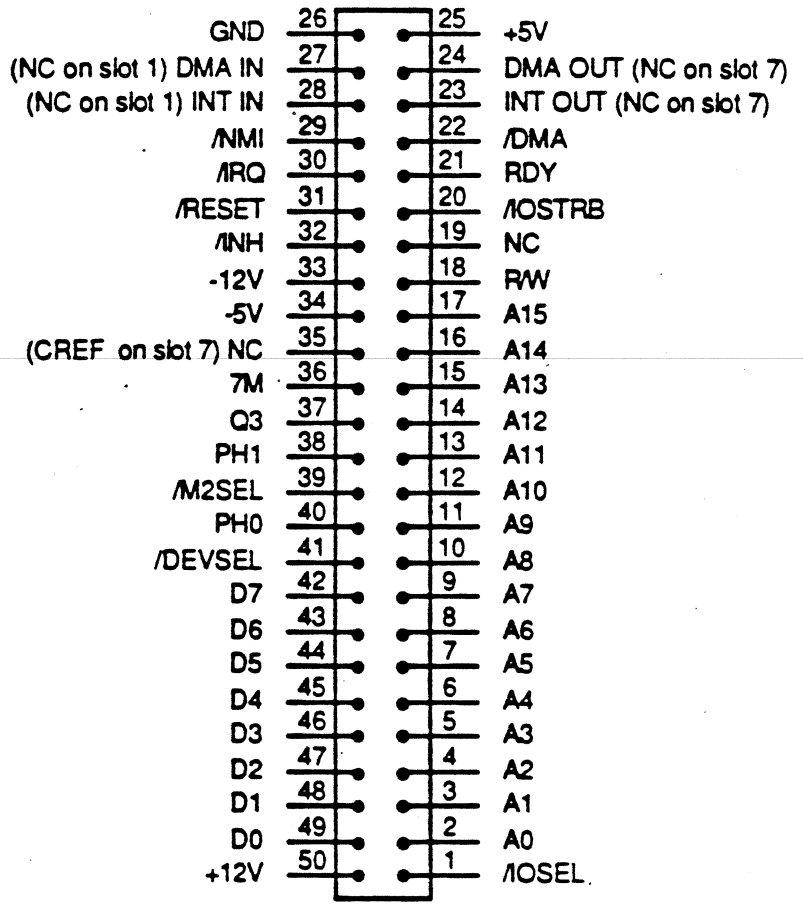
Apple Computer, Inc. - CONFIDENTIAL

The Cortland computer has seven I/O slots that are almost identical to the slots in the Apple //e, the only exception being /M2SEL which replaces µPSYNC on pin 39. The slots behave like their counterparts in the //e with only a few differences, the most important one being the behavior of the address bus . Since the Cortland computer can operate at 2.8 MHz and has a 24-bit address, the address bus to the slots is not always valid as it was in the //e. The signal /M2SEL indicates when a valid address for banks 224/225 (hex $E0/$E1) is present on the address bus and so should be used to qualify any address decoding that does not use one of the I/O enable lines.

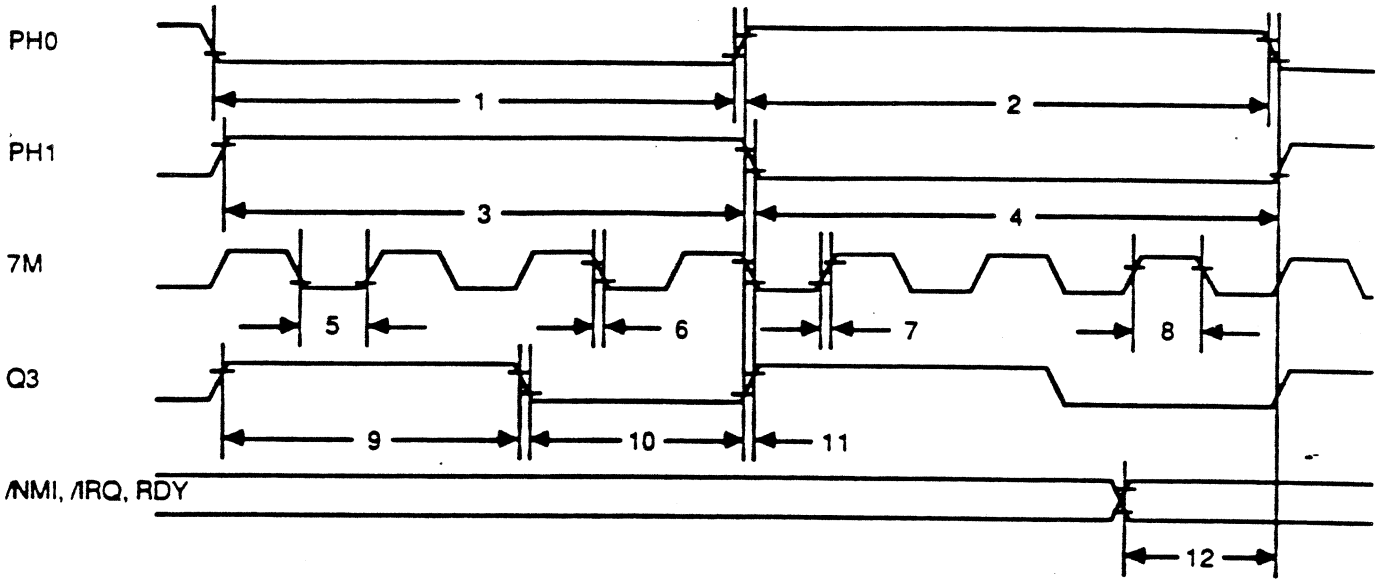
Cortland I/O Slot Pinout



The total current available for the 7 slots is 500 mA at +5V, 250 mA at +12V, 200 mA at -5V, and 200 mA at -12V.

The support circuitry for the slots is designed to handle a DC load of 2 LS TTL loads and an AC load of no more than 15 pF per pin per slot.

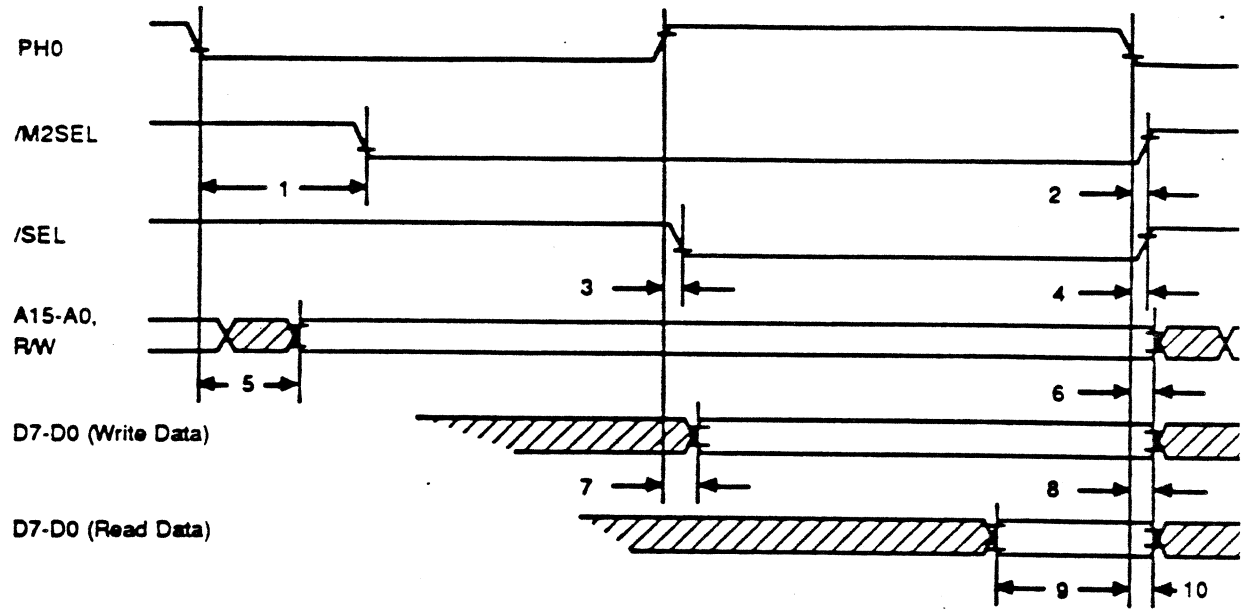
Slot I/O Clock and Control Signal Timing



Number	Description	Min(ns)	Max(ns)
1	PH0 low time	480	
2	PH0 high time	480	
3	PH1 high time	480	
4	PH1 low time	480	
5	7M low time	60	
6	Fall time, all clocks		10
7	Rise time, all clocks		10
8	7M high time	60	
9	Q3 high time	270	
10	Q3 low time	200	
11	Skew, PH0 to other clock signals	-10	10
12	Control signal setup time	140	

All of the clock signals present on the I/O slots are buffered by a custom I.C. called the "Slot Maker". As a result these signals are delayed somewhat from the corresponding signals on the main board. All of the timing parameters given here and with the other diagrams have been adjusted to account for this delay.

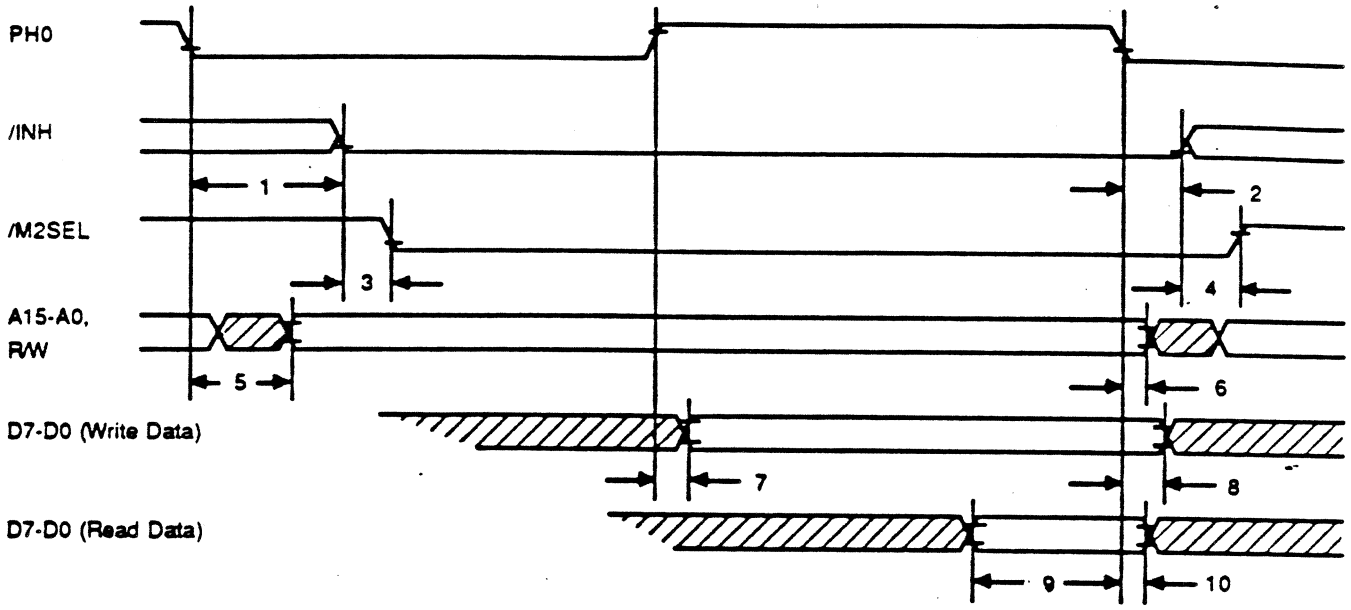
Slot I/O Read and Write Timing



Number	Description	Min(ns)	Ma
1	/M2SEL low from PH0 low		1
2	/M2SEL hold time	-10	
3	I/O enable low from PH0 high (/DEVn, /IOSELn, /IOSTRB)		
4	I/O enable high from PH0 low (/DEVn, /IOSELn, /IOSTRB)	10	
5	Address and R/W valid from PH0 low		1
6	Address and R/W hold time	15	
7	Write data valid delay		
8	Write data hold time	30	
9	Read data setup time to PH0	140	
10	Read data hold time	10	

The standard Cortland slot I/O timing is shown in the above diagram. When the computer is running in its high speed mode the address bus to the I/O slots is not valid entire PH0 cycle, and therefore, cannot be used to perform unqualified address decoc signal /M2SEL, which replaces the signal µSYNC, indicates when a slow, synchronize cycle is taking place and also shows when the value on the address bus will remain valid current PH0 cycle. This means that cards which use the Apple //e technique of "phantom put multiple I/O devices on one card must use /M2SEL to qualify their address decoding ci

I/O Read and Write Timing with /INH Active

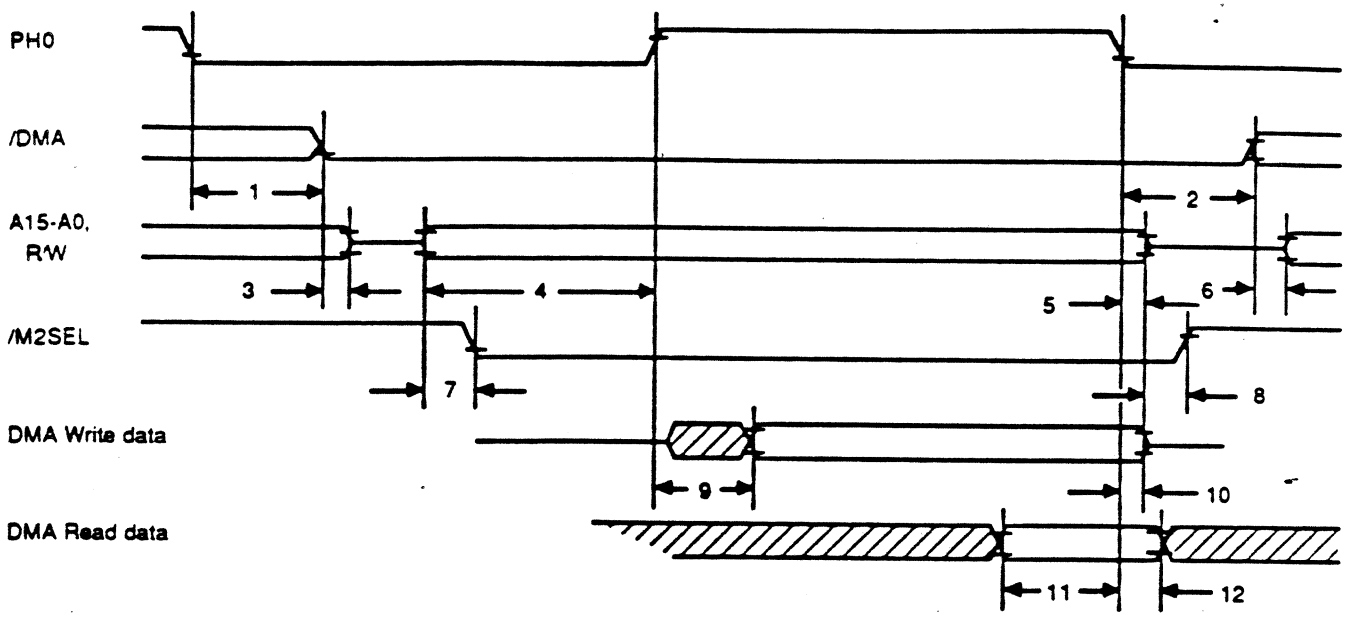


Number	Description	Min(ns)	Max(ns)
1	/INH valid after PH0 low		175
2	/INH hold time	15	
3	/INH low to /M2SEL low delay		30
4	/INH high to /M2SEL high delay		30
5	Address and R/W valid from PH0 low		100
6	Address and R/W hold time	15	
7	Write data valid delay		30
8	Write data hold time	30	
9	Read data setup time to PH0	140	
10	Read data hold time	10	

Read and write cycles that are directed to the I/O slots by /INH have the same timing parameters as normal I/O reads and writes. When /INH is asserted, the computer responds as if a MEGA // memory cycle were being performed.

Cards that use the /INH signal will only function properly if the computer is running in its slow mode (1 MHz). If the computer is running in its high speed mode, the addresses that are seen by cards in the I/O slots are not guaranteed to be valid during an entire PH0 cycle. Also, since the upper 8 bits of the memory address are not available to cards, the usefulness of /INH is greatly reduced in this machine.

/DMA Read and Write Timing



Number	Description	Min(ns)	Max(ns)
1	/DMA low from PH0 low		120
2	/DMA high from PH0 low		120
3	A15-A0 and R/W float from /DMA		30
4	DMA address and R/W valid before PH0 high	300	
5	DMA address and R/W hold time	10	
6	/DMA high to A15-A0 and R/W active		30
7	DMA address valid to /M2SEL low		30
8	DMA address float to /M2SEL high		30
9	PH0 high to write data valid		100
10	DMA write data hold time	10	
11	DMA read data setup time	125	
12	DMA read data hold time	30	

DMA devices will work if the Cortland computer is running slow, at 1 MHz. If the computer is running in its high-speed mode, at 2.8 MHz, DMA will work to the high-speed memory (banks 0 - 127) and will not work with the slow part of the system (all I/O and video memory). DMA can be performed to or from any part of the Cortland memory map, provided that the DMA Bank Register in the FPI is first set to the correct bank.